A Design Methodology for Temperature Variation Insensitive Low Power Circuits

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Outline

• Introduction
• Factor influencing MOSFET drain current (BSIM3V3 model)
• Device characteristics in temperature fluctuation
• Supply voltage optimization
• Temperature and voltage scaling effects on Low power applications
• Conclusion
• References
Introduction (1/3)

• Nominal supply voltage is not preferable for reliable circuit operation under temperature fluctuations.

• Optimizing the supply voltage for “temperature variation insensitive circuit performance” is presented.

• Challenges in IC design
  - Process Variation (static)
  - Environmental variation (dynamic)
  - Supply voltage
  - Temperature
  - Noise

• Frequency, leakage and power of dies are affected so that; functionality, performance, and revenue.

• Here we focus on temperature variations
Introduction (2/3)

• Imbalanced utilization and diversity of circuitry at different sections of an IC, cause temperature fluctuations within a die.

• Device, interconnects and communicating blocks performance can be affected.

• Device characteristics of MOSFETs, so performance of IC is affected.

• In a MOSFET model, there are many temperature dependent parameters such as mobility, threshold voltage, saturation velocity.

• All of them need to be modeled correctly.
Introduction (3/3)

• A bias voltage for which device parameter variations counterbalance each other’s effect on MOSFET current in temperature fluctuation.

• In an 180nm CMOS technology:
  – Optimum supply voltages for “temperature variation insensitive circuit performance”.
  – Minimum energy-delay product at different temperatures.
Factor influencing MOSFET drain current

- Temperature fluctuation has unique effects on MOSFET drain current.

- Drain current is the dominant parameter that determines circuit speed.

- Device parameters that are affected by temperature fluctuations, causing variations in drain current, should be defined.

- To characterize the drain current in deeply scaled nanometer devices, BSIM3v3 MOSFET equations are used.
BSIM3V3

- From the BSIM Group at the University of California at Berkeley.

- Latest industry-standard MOSFET model for deep-submicron digital and analog circuit designs

- Development of BSIM3v3 is based on Poisson's equation using gradual channel approximation and 2D analysis

- Device geometry and process parameters are included too.

- Brings robustness, accuracy and scalability for circuit simulation.

- BSIM3v3 model is used which includes the temperature effects, verified with measured data from room temperature up to +150 C.
BSIM3V3 Model for drain current

\[ I_{ds} = \frac{I_{dso}}{1 + \frac{R_{ds}}{V_{dseff}} I_{dso}} \]

Drain current with short channel effect
Parasitic drain to source resistance
Effective gate overdrive (Vgs - Vt)
Effective carrier mobility

\[ I_{dso} = \frac{\mu_{eff} V_{gsteff} (1 - A_{bulk} \frac{V_{dseff}}{2(V_{gsteff} + 2V_t)}) V_{dseff}}{[1 + V_{dseff} / (E_{sat}L_{eff})]} \]

Drain current of a long channel
Effective drain to source voltage
Thermal voltage
BSIM3V3 Model for mobility (1/2)

- Mobility, as a function of process parameters and bias condition by empirical formulations.

- All formulas contain $E_{eff}$

- $E_{eff}$ can be expressed as simply $(V_{gs} + V_{th}) / (T_{ox})$ in strong inversion.

- The effect of $V_{bs}$ and doping concentration are reflected in the $V_{th}$ term, the threshold voltage of the device.

- To describe the temperature effect of mobility, a second-order polynomial with parameters $U_a$, $U_b$ and $U_c$ being linear functions of the temperature is used in BSIM3v3.
BSIM3V3 Model for mobility (2/2)

\[
\mu_{eff} = \left[ \mu_0 \left( \frac{T}{T_{norm}} \right)^{U_{te}} \right] \left[ 1 + U_a(T)(V_{gstess} + 2V_{th})/T_{ox} + U_b(T)\left[ \frac{(V_{gsteff} + 2V_{th})}{T_{ox}} \right]^2 + U_c(T)V_{bs} \right]^{-1}
\]

where

\[
U_a(T) = U_a + U_{a1}(T/T_{norm} - 1)
\]
\[
U_b(T) = U_b + U_{b1}(T/T_{norm} - 1)
\]
\[
U_c(T) = U_c + U_{c1}(T/T_{norm} - 1)
\]

Are extracted from measured Id–Vgs characteristics at different Vbs

✓ Absolute value degrades as the temperature is increased. Drain current is lowered.
BSIM3V3 Model for “Vth”

- It decreases as temperature decreases due to Fermi-level and band gap energy shifts

- Vth depends linearly on the temperature over a wide range of temperature for the devices with a longer channel length.

\[ V_{th}(T) = V_{th}(T_{\text{norm}}, L, V_{ds}) + \left( K_{T1} + \frac{K_{T1}L}{L} + K_{T2}V_{bs} \right) \times \left( \frac{T}{T_{\text{norm}}} - 1 \right) \]

Threshold voltage at T\text{norm}  
Are extracted from experiments

- Absolute value degrades as the temperature is increased. Drain current is enhanced due to the increase in gate overdrive \((VGS-Vt)\).
BSIM3V3 Model for “Vsat”

- Saturation velocity is a weak function of temperature.

\[ v_{sat}(T) = v_{sat}(T_{norm}) - A_T \left( \frac{T}{T_{norm}} - 1 \right) \]

- Is extracted from measured Id–Vgs characteristics

- Absolute value degrades as the temperature is increased.
Device characteristics in temperature fluctuation

- For TSMC 180nm CMOS technology

<table>
<thead>
<tr>
<th>Supply Voltage (V)</th>
<th>Temperature (°C)</th>
<th>Gate Overdrive (V)</th>
<th>Carrier Mobility (x10^3 m^2/Vs)</th>
</tr>
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<tbody>
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<td></td>
<td>Variation (%)</td>
<td>5.37</td>
<td>4.95</td>
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<td>1.1</td>
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<td>-0.64</td>
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<td>Variation (%)</td>
<td>11.28</td>
<td>10.48</td>
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<tr>
<td>0.7</td>
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<td>Variation (%)</td>
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Variations in gate overdrive are smaller than carrier mobility variations when temperature is increased, carrier mobility degrades, so drain current and circuit speed are reduced.
Propagation delays

- Propagation delay variations with temperature at the nominal supply voltage.
- At the nominal supply voltage, the speed of circuits degrade by up to 19.6% as the temperature is increased from 25°C to 125°C.

✓ Nominal supply voltage is not preferable for reliable circuit operation under temperature fluctuations.
Supply voltage optimization (1/3)

- Supply voltage can be scaled to suppress the drain current variations due to temperature fluctuations.

- Sensitivity of gate overdrive to temperature fluctuations should be enhanced by lowering the supply voltage.

- At optimum supply voltage, the temperature fluctuation induced gate overdrive variation completely counterbalances the carrier mobility variation.

- At optimum supply voltage, transistor has insensitive constant drain current in temperature variation.
Supply voltage optimization (2/3)

They are similar

Electron mobility variation (NMOS) is higher than hole mobility variations (PMOS)

Supply voltage is scaled to a lower value in NMOS than in PMOS

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Supply voltage optimization (3/3)

- Temperature variation insensitive performance when operated at a supply voltage 45% to 53% lower than the nominal supply voltage (VDD = 1.8V)

- The optimum supply voltage of each CMOS circuit is within the range of the optimum supply voltages of the individual n-channel and p-channel devices.
Low power applications

- At optimum supply voltage, speed characteristics of an IC is insensitive to temperature fluctuations.

- It is lower than the nominal supply voltage.

- ICs operating at scaled supply voltages consume low power at the cost of reduced speed.

- This methodology is attractive in low power applications with relaxed speed requirements.
Energy delay product (EDP) (1/2)

- Low power designs aim at reducing power.
- A metric is needed to compare efficiencies. (power or energy)
- Power can be reduced by reduction of the operating frequency,
- The energy an operation requires can be reduced by lowering the supply voltage. Lower supply voltage increases the delay.
- “Delay/op * Energy/op” metric is used.
- Smaller “Energy-delay” means lower energy solution at the same level of performance (more energy efficient design).
- It is compromise between “energy consumption reduction” and “appropriate speed operation”.
EDP (2/2)

- For a CMOS gate, the dynamic power is: \[ P = aCV^2f \]

- If one operation per cycle is done, the energy per operation is: \[ E = aCV^2 \]

- The leakage current for a gate is: \[ I_t = W I_s e^{(V_{th}/V_o)} \]

- The leakage current for a complete chip is the sum of the leakage currents of all the gates

- The total energy per operation of a chip is:

\[
E = \sum_{i} a_i C_i V^2 + \sum_{i} W_i I_s e^{(V_{th}/V_o)} V T_c
\]

Each gate dissipates dynamic energy while it switches.  
Static energy is dissipated throughout the cycle.
Voltage scaling affects EDP

- Energy per operation can be reduced by lowering the power-supply voltage.
- Speed of the basic gates decreases with voltage scaling. (Capacitance and threshold voltages are constant, )

\[ t_d = k \frac{CV}{(V - V_{th})^2} \]

There is a minima at \( V_{dd} = 3V_{th} \). Around this point changing the supply voltage does not strongly affect EDP. Allowing one to trade delay for energy.
Temperature affects EDP (1/2)

- Energy/cycle and propagation delay is dependent on the die temperature.
- As the temperature increases:
  \[
  E = \sum_{i} a_i C_i V^2 + \sum_{i} W_i I_s e^{(V_{th}/V_o)} V T_c
  \]
  Static energy increases
- Propagation delay increases due to the degradation in carrier mobility.
- Circuits operation close to the nominal supply voltage, has the worst-case EDP @ the maximum temperature.
Temperature affects EDP (2/2)

The gate overdrive variations dominate the carrier mobility variations. Delay variation is determined by the variation of the gate overdrive. Reduction in the propagation delay dominates the increase in energy in the EDP term.

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- EDP at 25°C is higher than EDP at 125°C for the supply voltages below the optimum supply voltage.
- Worst case EDP is at a lower temperature for circuits operating at supply voltages below the optimum supply voltage.
**Conclusion**

- Tradeoffs in selecting the supply voltage (SV)

<table>
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<tr>
<th></th>
<th>SV for minimum EDP</th>
<th>SV for temperature variation insensitive circuit</th>
<th>Nominal SV</th>
<th>Having both conditions together</th>
</tr>
</thead>
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<td><strong>Energy</strong></td>
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<td>Energy per cycle is 59% to 82% lower than the energy per cycle at nominal SV</td>
<td>Energy per cycle is 71% to 81% lower than the energy per cycle at nominal SV</td>
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</tr>
<tr>
<td><strong>Speed</strong></td>
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<td>The circuit speed, as compared to the speed at nominal SV, degrades by up to 206% and 224%</td>
</tr>
<tr>
<td><strong>EDP</strong></td>
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<td></td>
<td>The minimum EDP is 23% to 47% worse than SV for min EDP.</td>
</tr>
<tr>
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<td>EDP is 20% to 45% better than EPD at nominal SV  → EDP is 6% worse than best EDP.</td>
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</tr>
</tbody>
</table>

- Low-power ICs can, also be made insensitive to temperature fluctuations with a modest amount of increase in EDP.
References (1/2)

• R. Kumar, V. Kursun, “A Design Methodology for Temperature Variation Insensitive Low Power Circuits”, Department of Electrical and Computer Engineering University of Wisconsin Madison, Madison, Wisconsin 53706-1691, Copyright 2006 ACM 1-59593-347-6/06/0004.


• W. Liu et al., BSIM3v3.2.2 MOSFET Model – User Manual, Department of Electrical and Computer Engineering, University of California, Berkeley, 1999.


References (2/2)


Q & A
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